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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,610	11/28/2001	Kuninori Kawabata	100353-00086	9276

7590 10/03/2003

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,610	KAWABATA ET AL.	
	Examin r	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication app ars on the c ver sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL ACTION

DETAILED ACTION

1. Applicants' Amendment has been entered and filed in August 10, 2003.

Response to Arguments

2. Applicant's arguments filed August 29, 2003 have been fully considered but they are not persuasive.

In the remarks, page 8, applicants submit that the cited prior arts fail to disclose or suggest at least the dynamic operating mode and static operating mode. The Office would like to point out that Furutani et al. clearly disclose the dynamic operating mode, in which equalize/precharge circuit is shown (fig. 1, circuit 2, dynamic operating mode in col. 5, lines 22 – 55), and static operating mode has been shown by Kurtze et al. (abstract), all of which establish grounds for the rejection set forth below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furutani et al. (US Pat 5,305,261) in view of Kurtze et al. (US Pat 6,022,004).

Regarding **claim 1**, Furutani et al. disclose a semiconductor device comprising:

signal lines over which signals are transferred (fig. 1, col. 17, lines 18 – 20, abstract: The semiconductor memory device further includes a load circuit

which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines.); and

a drive circuit driving the signal lines in operating modes (fig. 1, equalize/precharge circuit 2), the operating modes including a dynamic operating mode in which the signal lines are precharged (abstract, test and read modes are forms of dynamic modes and col. 5, lines 22 – 55).

Although Furutani et al. did not disclose a static operation mode in which the signal lines are not precharged, this feature is however shown by Kurtze et al. (abstract: A faster cycle type (e.g. page mode or static column) can thereby be employed in the Dynamic Random Access Memory (DRAM) memory by eliminating the DRAM precharge and RAS address portions of the cycle.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include this feature shown by Kurtze et al. to the invention of Furutani et al. so that memory with improved performance having faster cycle type is provided.

Regarding **claim 2**, Furutani further discloses a memory cell array (fig. 1, memory cell array 3) to which the signal lines are connected (signal lines IO in fig. 10), data read from the memory cell array being transferred over the signal lines (fig. 10, test data input 922 transferred over the signal lines).

Regarding **claim 3**, Furutani also discloses a test-dedicated line (col. 5, lines 10 – 12), a predetermined test of the semiconductor device being performed using the test-dedicated line and the signal lines (fig. 10, test data input 922 connect to signal lines).

Regarding **claim 4**, Furutani further discloses a circuit receiving the signal lines at inputs thereof and outputting a test result (fig. 10, line test circuit 5 outputs test result, shown error in figure), said test result and a logic level of the test-dedicated line forming a result of the predetermined test (dedicated test data line being wired-ANDed implies that its test output has to be a certain logical state).

Regarding **claim 5**, Furutani further discloses a precharge circuit precharging the signal lines and the test-dedicated line (abstract: the semiconductor memory device further includes a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines).

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furutani et al. in view of Sheppard (US Pat 4,388,705).

Regarding **claim 1**, Furutani et al. disclose a semiconductor device comprising:

signal lines over which signals are transferred (fig. 1, col. 17, lines 18 – 20, abstract: The semiconductor memory device further includes a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective

memory cell based on the potentials of the internal data transmitting lines.); and

a drive circuit driving the signal lines in operating modes (fig. 1, equalize/precharge circuit 2), the operating modes including a dynamic operating mode in which the signal lines are precharged (abstract, test and read modes are forms of dynamic modes and col. 5, lines 22 – 55).

Although Furutani et al. did not disclose a static operation mode in which the signal lines are not precharged, this feature is however shown by Sheppard (col. 4, lines 65 – 67).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include this feature shown by Sheppard to the invention of Furutani et al. for optimized response time for minimal signal margin.

Allowable Subject Matter

6. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicants are strongly suggested to review all of the cited references carefully for features relevant to the claims, more specifically, US Pat 4,878,101 (col. 6, lines 15 – 22) and US Pat 5,777,491 (col. 1, line 44 – col. 2, line 2).

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

10. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham

September 23, 2003

David Nelms
Supervisory Patent Examiner
Technology Center 2800